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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,709	08/28/2001	Michael K. Gschwind	YOR9-2001-0602 (8728-546)	5772
22150	7590	12/18/2006	EXAMINER CHOI, WOO H	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			ART UNIT 2189	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE 3 MONTHS		MAIL DATE 12/18/2006	DELIVERY MODE PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/940,709	GSCHWIND ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

1) Responsive to communication(s) filed on 26 September 2006.

2a) This action is **FINAL**.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

4) Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-37 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Withdrawal of Indication of Allowability***

1. Indication of allowability of claim 9 is withdrawn in view of the new reference (US Patent No. 6,868,472) made of record in this action.

### ***Claim Rejections - 35 USC § 112***

2. Claim 29 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not support the claimed configurable memory with three modes of operation where any one of the modes is selectable at any time based on comparing an address to an address range contained in a configuration register. The closest support for this claim is the first full paragraph on page 23 (lines 3 – 17). This paragraph discloses that “the access mode of the configurable memory is selected based upon the address.” The specification discloses only two modes of access for any given address - cache mode access and local memory mode access.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 8, 10 – 20, are rejected under 35 U.S.C. 102(e) as being anticipated by Kumar (US Patent No. 6,678,790).

5. With respect to claims 1 and 2, Kumar a memory system on a chip (figure 1), comprising:  
a configurable memory (12) having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (abstract), wherein the configurable memory comprises a memory array in which both tag bits (figure 2, 50) and data bits are stored in a single data line (col. 3, lines 32 – 33) in the memory array (figure 1, 12), in the second mode of operation, and

wherein a selection of any of the first mode of operation and the second mode of operation is capable of being overridden by another selection of an other of the first mode of operation and the second mode of operation (col. 2, lines 47 – 51).

6. With respect to claim 3, wherein the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a burn-in time (mode selection is under software control, making the mode selection possible anytime while the system is up and running, including “a burn-in time”, i.e. a period of initial operation of a new device).

7. With respect to claim 4, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected at a power-up time (col. 2, lines 51 – 55).
8. With respect to claim 5, the first mode of operation or the second mode of operation is selected at the power-up time using an external signal (col. 2, lines 51 – 55).
9. With respect to claim 6, the configurable memory is capable of having either the first mode of operation or the second mode of operation selected during a program execution (col. 2, lines 47 – 48).
10. With respect to claim 7, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of a special configuration register (col. 2, lines 47 – 48).
11. With respect to claim 8, the first mode of operation or the second mode of operation is selected during the program execution based upon a value of an external signal (col. 2, lines 48 – 51, control register is loaded by the CPU which is external to the memory).
12. With respect to claims 10 – 14, the configurable memory is **capable** of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses. (the claim only require a capability but not

actual mode setting based on the addresses, this only requires that the structure can switch modes and can compare addresses, both of which are taught by Kumar),

Dependent claims 11 – 14 relate to the capability discussed above.

13. With respect to claim 15, the configurable memory comprises:
  - a memory array (figure 2, 52); and
  - memory configuration logic for selecting the first mode of operation or the second mode of operation (figure 1, 16, figure 2, 58).
14. With respect to claim 16, the configurable memory is capable of selecting one of a local memory read mode and a local memory write mode in the first mode of operation and is further capable of selecting one of a cache read mode and a cache write mode in the second mode of operation (read mode, i.e. mode of operation while reading, and write mode, i.e. mode of operation while writing, are inherent in this type of memory, either in cache mode or local memory mode).
15. With respect to claim 17, the selection may be overridden by the other selection dynamically (col. 2, lines 47 – 51).
16. With respect to claim 18, the configurable memory comprises a plurality of static random access memory cells (col. 3, lines 34 – 35).

17. With respect to claim 19, the configurable memory comprises a plurality of dynamic random access memory cells (col. 3, lines 34 – 35).

18. With respect to claim 20, the configurable memory is capable of being dynamically employed as a sole memory (abstract, main memory) serving the processor and as a portion of a larger, memory hierarchy (abstract, cache, see also col. 1, lines 18 – 24, cache is a portion of a larger memory hierarchy that includes a cache memory and a main memory).

19. Claims 1 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Saulsbury (US Patent Publication No. 2002/0087821).

Saulsbury discloses a configurable memory that can be configured as a non-cache memory and a cache memory with tags bits and associated data bits in the memory array wherein both modes of operations are employed concurrently (page 7, paragraph 67)

20. Claims 1, 10 – 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Baltz (US Patent No. 6,321,318).

21. With respect to claims 1 and 10 – 14, Baltz discloses a memory system on a chip (abstract), comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (abstract), wherein the configurable

memory comprises a memory array (figure 9, 30, more specifically, 31 and 32) for storing tag bits and data bits in a single data line in the memory array, in the first mode of operation, wherein the configurable memory is **capable** of having either the first mode of operation or the second mode of operation selected based upon a result of comparing a supplied address to a range of addresses (claims only require a capability but not actual mode setting based on the addresses, this only requires that the structure can switch modes and can compare addresses, both of which are taught by Baltz, additionally, see col. 2, lines 38 – 46).

Dependent claims 11 – 14 relate to the capability discussed above.

22. With respect to claim 21, Baltz discloses that the first mode of operation and the second mode of operation are employed concurrently (col. 9, lines 9 – 10).

23. Claims 1 – 3, 6 – 10, 13 – 17, 20 – 23, 25, 26, 29, 30, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyake et al. (US Patent No. 6,868,472, hereinafter “Miyake”).

24. With respect to claims 1, 2, 6 – 10, 13 – 17, 20 – 23, 25, 26, 30, 33, and 34, Miyake discloses a memory system, comprising:

a configurable memory having a first mode of operation wherein the configurable memory is configured as a cache and a second mode of operation wherein the configurable memory is configured as a local, non-cache memory (col. 34, lines 40 – 50), wherein the configurable memory comprises a memory array for storing tag bits and data bits in a single data line in the memory array, in the first mode of operation (figure 8, 10),

wherein the first mode of operation or the second mode of operation is selected during the program execution based upon comparing a supplied address to at least one address range contained in at least one configuration register (col. 37, lines 7 – 26, 40 – 47, when RAM address region is supplied, the cache operates in the RAM mode).

25. With respect to claim 29, as shown above, Miyake's configurable memory supports, cache, RAM, and cache/RAM hybrid modes and uses address comparator to compare a supplied address to an address range stored in a register to select a mode of operation.

***Claim Rejections - 35 USC § 103***

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

27. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mikaye in view of Sample *et al.* (US Patent No. 6,377,912, hereinafter “Sample”), or in the alternative, in view of Natarajan (US Patent No. 6,611,796).

Miyake discloses all of the limitations of the parent claim as discussed above. However, Miyake does not specifically disclose macro cells to implement memory system. On the other

hand, Sample (col. 29, lines 11 – 17, col. 31, lines 27 – 33) and Natarajan (col. 4, lines 16 – 23) disclose the use of macro cells in IC memory chip designs.

It would have been obvious to one of ordinary skill in the art, having the teachings of Miyake and Sample or Natarajan before him at the time the invention was made, to use the design techniques using macros teachings of Sample or Natarajan in the design of Miyake's system, in order to be able to verify electronic circuit designs before fabrication (Sample 16 – 18, Natarajan 23 – 26).

28. Claims 27, 28, 31, 34 - 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake in view of Isaak (US Patent No. 6,426,549).

Miyake discloses all of the limitation of the parent claim as discussed above. However, Miyake does not specifically disclose methods of integrating the claimed memory package using a chip stack and a flip chip techniques. On the other hand, Isaak discloses both of these techniques (abstract).

It would have been obvious to one of ordinary skill in the art, having the teachings of Miyake and Isaak before him at the time the invention was made, to use the IC packaging teachings of Isaak to make the configurable memory IC of Miyake, in order to be able to actually produce the memory devices. Isaak's method uses available materials and known process techniques and is suitable for automated production methods (col. 3, lines 49 – 53).

***Response to Arguments***

29. Applicant's arguments regarding Kumar and Balz references with respect to claim 1 have been fully addressed in the Response to Argument section of the last action mailed June 23, 2006.

Applicant's other arguments are moot in view of the new grounds of rejections.

***Conclusion***

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Woo H. Choi  
December 11, 2006